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EXAMINER	
SLUTSKER, JULIA	

ART UNIT	PAPER NUMBER
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/572,799	LEDERER ET AL.	
	Examiner	Art Unit	
	JULIA SLUTSKER	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,24,26-34 and 36-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22,24,26-34 and 36-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 20-22, 24, and 26-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auberton-Herve (US 2003/0129780) in view of Applicant Admission of the Prior Art (AAPA) and Inoue (EP 104452 A1).

Regarding claims 20, Auberton-Herve teaches a method of manufacturing of a multilayer semiconductor structure and a multilayer semiconductor structure comprising a silicon substrate (Fig.5c, numeral 3), an active semiconductor layer (Fig.5c, numeral 10) and an insulating layer (Fig.5c, numeral 16), wherein the method comprises forming the intermediate layer by depositing an amorphous silicon layer (Fig. 5, numeral 6) which is located between the silicon substrate (Fig.5, numeral 2) and the insulating layer (Fig. 5, numeral 16) in order to increase the charge trap density between the insulating layer and the high resistivity silicon substrate, thereby suppressing ohmic losses inside the high resistivity silicon substrate (note: " in order to increase… " is a intended outcome recitation rather than the required step further limiting the scope of the claims. The applied prior art can be so modified or used and therefore renders unpatentable such claims. See, for example, M.P.E.P. § 2111.04, and precedents cited therein.)

Auberton-Herve does not disclose (1) that the silicon substrate has a resistivity higher than 3K. Ω.cm; and (2) crystallizing the amorphous silicon layer to form a polycrystalline layer.

Regarding element (1) AAPA however discloses the use of high-resistivity substrates with resistivity higher than 3K. Ω.cm (Spec., page 2, lines 15-22).

It would have been therefore obvious to one of ordinary skill in the art at time the invention was made to modify Auberton-Herve reference by combining with AAPA to have the silicon substrate with a resistivity higher than 3K. Ω.cm for the purpose of reducing losses and coupling in high-frequency applications (Spec., page 2, lines 16-22).

Regarding element (2), Auberton-Herve discloses that the intermediate layer contains polysilicon layer (Fig.5, numeral 5). And Inoue discloses that the effective method of forming polysilicon layer is by crystallizing deposited amorphous silicon on the silicon substrate and crystallizing the amorphous silicon so as to form the polysilicon layer (column 13, [0085], [0087]).

It would have been therefore obvious to one of ordinary skill in the art at time the invention was made to modify Auberton-Herve with Inoue and to crystallizing the amorphous silicon so to form the polysilicon for the purpose of effective formation of polysilicon layer and decreasing of damage during ion implantation (Inoue, column 20[0088]).

Regarding claim 21, Auberton-Herve discloses that the intermediate layer comprising grains having a size, wherein the mean size of the grains of the intermediate

layer is smaller than 150 nm (implicit in page 5, [0084], [0085], note: thickness of the polycrystalline layer in Fig.1, 50 nm (page 5, [0088])).

Regarding claims 22, Auberton-Herve does not disclose that the intermediate layer has a charge trap density of at least 10^{12}/cm2/eV.

However, it would have been obvious to one of ordinary skill in the art at time the invention was made to adjust the charge trap density to at least 10^{12}/cm2/eV for the purpose of increasing efficiency of the gettering layer.

Regarding claims 24, Auberton-Herve discloses that the intermediate layer having an RMS roughness, wherein the RMS roughness of the intermediate layer has an average value smaller than or equal to 0.5 nm (it has been disclosed that the intermediate layer (Fig.5, numerals 5,6 consist of a polycrystalline material (numeral 5) covered with amorphous silicon (numeral 6) to obtain a surface with very low roughness (page 6, [0115], page 7, [0123], [0127]).

Regarding claim 26, Inoue discloses that crystallizing comprises any of thermal annealing or rapid thermal annealing (RTA) or laser crystallization (column 19, [0085]).

Regarding claims 27, Auberton-Herve discloses bonding (Fig.5 a to b) an intermediate layer-covered high resistivity silicon substrate (Fig.5, numeral 3) to an insulator-passivated semiconductor substrate (Fig.5, numeral 12).

Regarding claim 28, Auberton-Herve discloses oxidation of a surface of the intermediate layer prior to bonding the high resistivity silicon substrate to the insulator-passivated semiconductor substrate (page 5, [0074], polishing).

Regarding claim 29, Auberton-Herve discloses providing an intermediate layer (Fig.5, numeral 5,6) on an insulator-passivated semiconductor substrate (Fig.5, numeral 3), and bonding the intermediate layer insulator-passivated semiconductor to a high-resistivity silicon substrate (Fig.5, numeral 12).

Regarding claim 30, Auberton -Herger discloses that the intermediate layer has a layer thickness of at least 100 nm (page 5, [0092]).

Regarding claim 31, Auberton-Herve does not disclose that the density of charge traps remains higher than or equal to 10^{11}/cm2/eV.

However it would have been obvious to one of ordinary skill in the art at time the invention was made to have density of charge traps remains higher than or equal to 10^{11}/cm2/eV.

3. Claims 32, 33, 36-43, 45-48, 51-57, and 59-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auberton-Herve (US 2003/0129780) in view of Applicant Admission of the Prior Art (AAPA).

Regarding claim 32, Auberton-Herve discloses a multilayer structure comprising a silicon substrate (Fig.5c, numeral 3), an active semiconductor layer (Fig.5c, numeral 10) and an insulating layer (Fig.5c, numeral 16) in between the silicon substrate and the active semiconductor layer, wherein the multilayer structure comprises an intermediate layer (Fig.5a, numerals, 5, 6) being a re-crystallized polysilicon layer (Fig.5, numeral 5; note: "being a re-crystallized polysilicon layer" is an product by process recitation. "Even though product-by-process claims are limited by and defined by the process determination of patentability is based on the product itself. The patentability of a

product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985) (see MPEP 2113). In the present case, since Auberton-Herve discloses polysilicon layer (Fig.5, numeral 5), it anticipated this limitation) in between the high resistivity silicon substrate and the insulating layer, the intermediate layer comprising grains having a size, wherein the mean size of the grains of the intermediate layer is smaller than 150 nm (implicit in page 5, [0084], [0085], note: thickness of the polycrystalline layer in Fig.1, 50 nm (page 5, [0088]) ; since the thickness of the layer is 50 nm, that the grain size could not be larger than 50nm).

Auberton-Herve does not disclose that the silicon substrate has a resistivity higher than 3KΩ.cm. However, AAPA discloses the use high-resistivity substrates with resistivity higher than 3K. Ω.cm (Spec., page 2, lines 15-22).

It would have been therefore obvious to one of ordinary skill in the art at time the invention was made to modify Auberton-Herve with AAPA to have the silicon substrate with a resistivity higher than 3KΩ.cm for the purpose of reducing losses and coupling in high-frequency applications (Spec., page 2, lines 16-22).

Regarding claim 45, Auberton-Herve discloses a method of manufacturing of a multilayer semiconductor structure comprising a silicon substrate (Fig. 5, numeral 2) and an active semiconductor layer (Fig.5, numeral 10) and an insulating layer (Fig.5, numeral 16) in between the silicon substrate (Fig.5, numeral 2) and the active

semiconductor layer (Fig.5, numeral 10), wherein the method comprises: introducing an intermediate layer (Fig.5, numerals 5, 6) between the silicon substrate (Fig.5, numeral 2) and the insulating layer (Fig.5, numeral 16) in order to increase the charge trap density between the insulating layer and the silicon substrate, thereby suppressing ohmic losses inside the high resistivity silicon substrate (note: " in order to increase… is a intended outcome recitation rather than the required step further limiting the scope of the claims), the intermediate layer (Fig.5, numerals 5, 6) being formed in contact with the silicon substrate (Fig.5, numeral 2) and the insulating layer (Fig.5, numeral 16), wherein applying the intermediate layer comprises applying any of an undoped or lightly doped silicon layer, an undoped polysilicon layer ([0084], [0085]).

Auberton-Herve does not disclose that the silicon substrate has a resistivity higher than 3KΩ.cm. However, AAPA discloses the use high-resistivity substrates with resistivity higher than 3K. Ω.cm (Spec., page 2, lines 15-22).

It would have been therefore obvious to one of ordinary skill in the art at time the invention was made to modify Auberton-Herve with AAPA to have the silicon substrate with a resistivity higher than 3KΩ.cm for the purpose of reducing losses and coupling in high-frequency applications (Spec., page 2, lines 16-22).

Regarding claim 56, Auberton-Herve discloses multilayer structure comprising a silicon substrate (Fig.5, numeral 2), an active semiconductor layer (Fig.5, numeral 10) and an insulating layer (Fig.5, numeral 16) in between the silicon substrate and the active semiconductor layer, wherein the multilayer structure comprises an intermediate layer (Fig.5, numerals 5, 6) in between the silicon substrate and the insulating layer, the

intermediate layer comprising grains having a size, wherein the mean size of the grains of the intermediate layer is smaller than 150 nm (implicit in page 5, [0084], [0085], note: thickness of the polycrystalline layer in Fig.1, 50 nm (page 5, [0088]) ; since the thickness of the layer is 50 nm, that the grain size could not be larger than 50nm) , the intermediate layer being in contact with the silicon substrate and the insulating layer, wherein the intermediate layer consists of any of an undoped or lightly doped silicon layer, an undoped polysilicon layer ([0084], [0085]).

Auberton-Herve does not disclose that the silicon substrate has a resistivity higher than 3KΩ.cm. However, AAPA discloses the use high-resistivity substrates with resistivity higher than 3K. Ω.cm (Spec., page 2, lines 15-22).

It would have been therefore obvious to one of ordinary skill in the art at time the invention was made to modify Auberton-Herve with AAPA to have the silicon substrate with a resistivity higher than 3KΩ.cm for the purpose of reducing losses and coupling in high-frequency applications (Spec., page 2, lines 16-22).

Regarding claims 33, 40, 43, 47, and 57, Auberton-Herve does not disclose that the intermediate layer has a charge trap density of at least 10^{12}/cm2/eV.

However, it would have been obvious to one of ordinary skill in the art at time the invention was made to adjust the charge trap density to at least 10^{12}/cm2/eV for the purpose of increasing efficiency of the gettering layer.

Regarding claims 36, 48, and 59, Auberton-Herve discloses that the intermediate layer having an RMS roughness, wherein the RMS roughness of the intermediate layer has an average value smaller than or equal to 0.5 nm (it has been disclosed that the

intermediate layer (Fig.5, numerals 5,6 consist of a polycrystalline material (numeral 5) covered with amorphous silicon (numeral 6) to obtain a surface with very low roughness (page 6, [0115], page 7, [0123], [0127]).

Regarding claims 38 and 61, Auberton-Herve discloses that the insulating layer is formed of at least one of an oxide (page 6, [0112]).

Regarding claims 51, Auberton-Herve discloses bonding (Fig.5 a to b) an intermediate layer-covered high resistivity silicon substrate (Fig.5, numeral 3) to an insulator-passivated semiconductor substrate (Fig.5, numeral 12).

Regarding claim 52, Auberton-Herve discloses oxidation of a surface of the intermediate layer prior to bonding the high resistivity silicon substrate to the insulator-passivated semiconductor substrate (page 5, [0074], polishing).

Regarding claim 53, Auberton-Herve discloses providing an intermediate layer (Fig.5, numeral 5,6) on an insulator-passivated semiconductor substrate (Fig.5, numeral 3), and bonding the intermediate layer insulator-passivated semiconductor to a high-resistivity silicon substrate (Fig.5, numeral 12).

Regarding claim 41, 42, and 54, Auberton -Herve discloses that the intermediate layer has a layer thickness of 300 nm (page 5, [0092]).

Regarding claims 39 and 46, Auberton-Herve teaches increasing charge trap density comprises applying an intermediate layer (Fig.5a, numerals, 5, 6) in between the silicon substrate and the insulating layer, the intermediate layer comprising grains having a size, wherein the mean size of the grains of the intermediate layer is smaller

than 150 nm, (implicit in page 5, [0084], [0085], note: thickness of the polycrystalline layer in Fig.1, 50 nm (page 5, [0088])).

Regarding claim 55, Auberton-Herve does not disclose that the density of charge traps remains higher than or equal to 10^{11}/cm2/eV.

However it would have been obvious to one of ordinary skill in the art at time the invention was made to have density of charge traps remains higher than or equal to 10^{11}/cm2/eV.

Regarding claims 37 and 60, Auberton-Herve discloses that the active semiconductor layer is made from at least of Si (page 6, [0109]).

4. Claims 34, 44, and 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Auberton-Herve (US 2003/0129780) in view of Applicant Admission of the Prior Art (AAPA) as applied to claims 32 and 56 above, and further in view of Shiota et al (EP 0975011 A, hereinafter "Shiota").

Regarding claims 34, 44, and 58 , the combination of Auberton-Herve and AAPA does not disclose that the multilayer structure has an effective resistivity higher than 5KΩCm. However, Shiota teaches that the multilayer structure has an effective resistivity higher than 10KΩCm (column 13, [0108], column 17, [0143]).

Thus, it would have been obvious to one of ordinary skill in the art at time the invention was made to modify combination of Auberton-Herve and AAPA to have the multilayer structure has an effective resistivity higher than 10KΩCm as taught by Shiota for the purpose reducing losses and coupling in high-frequency applications (AAPA, Spec., page 2, lines 16-22).

5. Claim 49 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auberton-Herve in view of Applicant Admission of the Prior Art (AAPA) as applied to claim 45 above, and further in view of Inoue (EP 104452 A1).

Regarding claim 49, Auberton-Herve in view of AAPA discloses all limitations of claim 24 for reasons above. Auberton-Herve in view of AAPA does not teaches that applying a polysilicon layer comprises depositing amorphous silicon on the silicon substrate and crystallizing the amorphous silicon so as to form the polysilicon layer.

Auberton-Herve however discloses that the intermediate layer contains polysilicon layer (Fig.5, numeral 5). And Inoue discloses that the effective method of forming polysilicon layer by crystallizing deposited amorphous silicon on the silicon substrate and crystallizing the amorphous silicon so as to form the polysilicon layer (column 13, [0085], [0087]).

It would have been therefore obvious to one of ordinary skill in the art at time the invention was made to modify Auberton-Herve with Inoue and to crystallizing the amorphous silicon so to form the polysilicon for the purpose of effective formation of polysilicon layer and decreasing of damage during ion implantation (Inoue, column 20[0088]).

Regarding claim 50, in the combination above, Inoue teaches that crystallizing comprises any of thermal annealing or rapid thermal annealing (RTA) or laser crystallization (column 19, [0085]).

Response to Arguments

6. Applicant's arguments with respect to claims 20-22, 24,26-34, 36-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIA SLUTSKER whose telephone number is (571)270-3849. The examiner can normally be reached on Monday-Friday, 8 a.m.-5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Keisha Rose can be reached on (571)-272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS
July 22, 2009

/Asok K. Sarkar/
Primary Examiner, Art Unit 2891
August 3, 2009